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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,918	10/21/2003	Michael M. Klock	NVID-061/00US	6921

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EXAMINER	
WOODS, ERIC V	

ART UNIT	PAPER NUMBER
2628	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/690,918	KLOCK ET AL.	
	Examiner	Art Unit	
	Eric Woods	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22,24-27 and 33-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22,24-27 and 33-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/2/2007 has been entered.

Response to Arguments

Applicant's arguments, see Remarks pages 5-6 and claim amendments, filed 4/2/07, with respect to the rejection(s) of claim(s) 1-32 under various grounds have been fully considered and are persuasive.

Claims 1-21, 23, and 28-32 are cancelled, therefore rendering all rejections against those claims moot.

Claims 33-35 have been added.

Therefore, in view of applicant's amendments to the claims, the rejection of claims 22 and 24-27 has been withdrawn.

Applicant's arguments are therefore moot, since all grounds of rejections against the claims stand withdrawn.

However, upon further consideration, a new ground(s) of rejection is made in view of various references as set forth below.

The following point(s) are discussed in regards to the grounds of rejection under 35 USC 103(a) concerning substitutes, motivation / rationale, and related issues.

It is respectfully pointed out that, as clearly set forth in MPEP 2105-2106, any element, step, or functionality that is implemented by hardware can be implemented as and via software, and vice versa. Additionally, as noted therein, implementing functionality in one or the other is a well-known expedient, e.g. a matter of designer preferences.

Further, with respect to claim 22, it is further duly noted that the recited GPU contains a graphics pipeline, but that the other components, including an 'overclocking control module,' could be implemented using software – see as evidence claim 24, which recites in part, "The graphics system of claim 22, wherein said graphics system includes **computer executable instructions** for running a ... program having an **overclocking control module** for selecting and evaluating overclocking parameters ..." (It being further noted, as in the last Office Action, that the applicant released a software utility called CoolBits in excess of the time period set forth under 35 USC 102(b) for eligibility that performed similar functionality to that of Bigjakkstaffa)

This would be further evidence that the control module could be software or firmware.

Extensive previous discussion can be found in previous Office Actions concerning the reasons and rationale for why automating a task previously done manually would be an obvious expedient, see e.g. Response to Arguments section in

Final Office Action mailed 12/01/2006 (refer to 82 USPQ2d 1385). Such discussion is herein incorporated by reference in its entirety.

Examiner has clearly stated and shown in previous Office Actions (most recently 12/06/2006) and evidence (see Gasior reference, provided to applicant on 2/23/2005)-- and applicant has not argued otherwise before the close of prosecution (twice) -- that the NVIDIA GeForce4 Ti 4200 video card inherently has a graphic pipeline, thusly effecting MPEP 2173.02 [R-5], last paragraph.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 24 stands rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 24 recites the limitation "the overclocking control module" in line 1. There is insufficient antecedent basis for this limitation in the claim; that is, the parent claim already has an overclocking control module.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 22 and 24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Bigjakkstaffa (http://www.sysopt.com/articles/VCOGuide/) ('B1') in view of Fox (US 6,340,972 B1)('F1') in view of Baggs (US PGPub 2002/0164084 A1)('B2').

As to claim 22,

B1 teaches:

A graphics system, comprising: (B1 pages 1-4)

-A graphics processing unit (GPU), comprising: (B1, page 2, NVidia GeForce4 Ti 4200)

-A graphics pipeline; and (B1 inherently possesses a graphic pipeline; this fact has been previously established)

-A clock controller to control a GPU clock signal generator and a memory clock generator; and (B1 – page 3; B1 allows user to adjust Core clock rate and Memory clock rate; therefore, B1 must inherently possess a clock controller that is operative to control a GPU clock rate and (a controller for) a memory clock rate that is receptive to adjustment remotely, e.g. by a

software application)

B1 does not expressly teach, but F1 teaches:

-An overclocking control module disposed in said GPU configured to evaluate overclocking parameters in response to a function call received by the GPU, the overclocking control module including: (F1, 2:8-20, within lighting unit 32, element 50, Figure 3, control module, controls: graphics pipeline 57 (e.g. GPU) and storage section 51, accumulator 51 (e.g. memory) via function call from graphics application (GPU) – **50 is operable to control clock rate of 52, control operation of 55, 51** – see 3:25-59, where this is specified by application to control module)

B1 teaches **implementing a stress test that includes executing a graphics test sequence in said pipeline for selected overclocking parameters and monitoring errors of said graphics pipeline** (B1 page 8, incremental adjusting and benching each set of parameters, user observes if unusual graphical glitches, e.g. errors, appear (textures flicker, colored dots appearing, etc) indicating instability), but B1 and F1 fail to teach a **graphics pipeline stress tester in said GPU** (B1 utilizes the user).

Baggs teaches an **artifact detector 400** that **detects errors (artifacts) in an image** (Abstract, [0066]) by performing statistical tests.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify B1 in light of F1 to allow the presence of a control unit that can adjust the clock rates of all components (e.g. GPU / pipeline and memory) on the graphics card by the user because such a modification enables the system to be more easily fabricated (e.g. one controller vs. two, fewer requirement wires, traces and lower transistor count), to operate more efficiently (lower power)(Abstract, 9:1-10), and to be more flexible with respect to user requests (Abstract, 2:8-20, 9:1-10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the (B1 modified in view of F1) system to utilize the artifact detector of B2 to detect and count the number of errors in the video stream instead of having the observer perform such a function (as in B1 and in 5,313,280 to Strauss) because it allows the objective measurement of the total quantity of errors on a per-frame basis and is more accurate in doing so than a human observer because it examines / tests regions of the screen at a closer level than a human observer could at a much higher rate of speed. It is further a well-known expedient to modify a system to perform automatically a task previously performed by a human being (see Response to Arguments, MPEP 2144.04(III) [R-1], and 82 USPQ2d 1385). Also, it would have been obvious that such functionality as stress testing, etc, could be carried out by the software in B1 for the reasons set forth in the Response to Arguments above.

With regards to claim 24, clearly the overclocking menu tab on B1 page 3, and B1 page 5, first paragraph, wherein the user requests overclocking by ticking the

checkbox marked "Enable driver level hardware overclocking" near the top of the window of the overclocking control panel) and wherein said user inputs said request to said control panel (see Bigjakkstaffa wherein the graphical user interface that the user is interacting with is inherently generated by computer executable instructions, and discusses adjusting in 15MHz increments – page 8).

With regards to claims 25 and 26, B1 page 8 teaches determining a maximum safe GPU and memory clock rate (e.g. the point at which pixel errors exceed a threshold) on page 8, etc.

With regards to claim 27, this merely combines determining the maximum clock rates of the GPU and memory, both of which are shown in B1, where both are optimized.

Claim 33 is rejected under 35 USC 103(a) as unpatentable over B1, F1, B2 as applied to claim 22, and further in view of Feierbach (US PGPub 2001/0009022 A1)('F2') and Cooper (US PGPub 2002/0143488 A1)('C1').

As to claim 33, B1 clearly teaches a personal computer, which inherently contains a **CPU coupled to the GPU over a bus.** Clearly, B1 utilizes **driver programs** as on page 8 and as discussed above with respect to claim 24. The rejections of claims 22 and 24 are incorporated herein by reference in their entirety.

B1/F1/B2 fails to expressly teach the use of automatic testing of sets of parameters and then determining if a set of overclocking parameters passes said stress test if the number of pixel errors is below a threshold level. B1 specifically does teach

(page 8) that the number of visual tears is counted to find the point where the speeds are too high, which could be regarded as a threshold, and as modified by F1/B2 clearly tests a set of overclocking parameters (e.g. memory/ processor clock speed pairs.)

In the memory arts, F2 teaches the use of a binary test pattern being written to a DRAM. **Initial or default values** (e.g. **initial starting point**) are chosen for the variable(s) that are not optimized, but one variable is set to an aggressive (e.g. high) value (e.g. step 50, Figure 2) [0007,0013]. If the test pattern is read from the DRAM and there are no errors, e.g. it matches the original binary test pattern [0015] (steps 51-53), then the system proceeds to determine if the opposite test pattern can be held (steps 54-56)[0016-0018]. If so, then the system scales the value to a higher one (step 59)(if the loop is on the first pass). If at any point an error is detected, the system goes into a loop check mode, where the aggressively scaled value is decreased (see path step 66). However, if the resolution is less than a predetermined resolution threshold from the **calculated upper refresh period limit (e.g. maximum end point),** then the system passes that stable value on to the registers for use [0018-0024], the procedure is illustrated in Figures 3(a)-(e). This procedure constitutes **a set of supported overclocking parameters**. This procedure is then used to determine optimal values for the other parameters [0028] - that is, scaling the values up from the initial to an optimal level, and/or scaling them down to an optimal level. These techniques are applicable to **DRAM clock rates**, in that the signals being adjusted are generated by control circuits that have **system clocks** therein [0006] (**e.g. memory clock rate**). Therefore, adjusting the system clocks is clearly in keeping with the spirit of the invention [0029].

The F2 reference teaches testing of each the three parameters separately (RAS, CAS, and refresh rates) and finding the maximum safe or stable values for each reference (**e.g. evaluating set of overclocking parameters**). Therefore, in light of the teachings of F2, It would have been obvious to one of ordinary skill in the art at the time the invention was made to optimize each variable (clock rate) and to set them all to their maximum safe values (as per F2). F2 further teaches setting all of the variables (RAS, CAS, refresh rate) to their maximum safe values. F2 clearly teaches the use of automatic testing for parameter sets with respect to memory speed, and checking to see if a set of overclocking parameters passes said stress test. That is, F2 teaches an automated method of scaling memory clock rates (e.g. CAS / RAS are created from system clock rates) and testing them to find the optimal values, and tests sets of parameters to find the optimal set.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify B1/F1/B2 to use the techniques of F2 to utilize automatic testing of **parameter sets for memory clock rate** to achieve the lowest power consumption (e.g. longer intervals between refreshes) and more efficient use of memory.

C1 clearly teaches **automatically stress testing a processor** over different sets of **memory and processor parameters**. Specifically, C1 teaches that a system has a maximum safe operating temperature [0003] ('junction temperature specification')[0029](wherein if the temperature exceeds said safe limit, damage will occur to the chip). C1 teaches that thermal sensors can be on-die [0031](e.g. junction

temperature monitors)('maximal allowable die temperatures'). The system of C1 (Figure 3, stress tests – including graphics controller to graphics controller or graphics controller to local memory – [0035-0036]) very clearly tests different clock-frequency / bandwidth (e.g. bus speed) combinations (Abstract).

C1 also teaches the use of graphics stress software to determine maximum bandwidths and speed (fill rates, etc), wherein such stress tests and the instant embodiments can be applied upon graphics controllers and the like (e.g. GPUs), wherein this clearly must require automatically running benchmarks to obtain information such as maximum fill rate and the like. Figure 6 also shows such stress tests.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify B1/F1/B2/F2 in light of the teachings of C1 because they allow easier, more direct visualization of test results, temperature versus speed and bandwidth plots, etc, wherein such can be displayed as a GUI [0027,0033,0040], wherein this use of a GUI and the system of C1 increases efficiency and requires minimal customer input or direction, etc [0040], again with the integral sensors being the most effective [0039] (as in within the GPU).

Claim 34 are rejected under 35 USC 103(a) as unpatentable over B1, F1, B2, F2, and C1 as applied to claim 1 and further in view of Culbert et al (US PGPub 2005/0049729 A1)('C1').

As to claim 2, B1 clearly suggests adding a fan to the GPU to ensure effective cooling (page 8), but does not teach changing the fan speed.

C2 clearly teaches such limitations in [0011-0013], in that when the processor (inclusive of GPU) speed changes, the fan speed will change as well, as in [0041], where the CPU voltage and frequency control are provided to have many states, wherein the cooling fans have speed control as well, as dependent upon processor speed and the temperature as required [0069, 0096]. The thermal manager keeps the components under a desired temperature by controlling fan speed, and the like. It would have been obvious to one of ordinary skill in the art to modify B1, F2, B2, F1, and C1 to vary fan speed with increases in processor speed and decrease it with decreases therein because the heat produced will be greater or lesser as the case may be above because such variance increases cooling and helps keep the processing unit(s) under the goal (maximum) temperature, thusly allowing better load testing a la C1.

Claim 35 is rejected under 35 USC 103(a) as unpatentable over B1, B2, F1, F2, and C1 as applied to claim 33 above and further in view of C2 and Kao (US 6,622,254)('K1').

As to claim 5, B1, B2, F1, F2, and C1 collectively teach adjusting memory timings, wherein the CAS / RAS rates of DRAM are derived from system clocks found within the memory module (see C1 as above), and adjusting the memory clock frequency would obviously change the system clocks generating aforementioned, thusly changing the memory timings. They further teach adjusting at least one clock rate to

form at least one new clock rate, as discussed in the rejection to claim 33, which is incorporated by reference.

B1, B2, F1, F2, C1 fail to expressly teach setting a chip voltage, memory timing, and fan speed for each said at least one new clock rate.

C2 very clearly teaches that the processor has various states that include both chip voltages and frequencies (e.g. state 1 has frequency 1 and voltage 1). C2, as in the rejection to claim 2 above, clearly teaches varying fan speeds based on processor operating conditions.

Therefore, as noted above, a given processor operating frequency will have a linked operating voltage (e.g. higher operating frequency requires more power) as per the teachings of C2. Concomitant with higher power usage, the thermal load of the GPU or CPU will increase, thusly necessitating a higher fan speed associated with a state having higher operating frequency (supported by B1 on page 8, given that a fan is required to attempt overclocking). Motivation and rationale for this modification are taken from the rejection to claim 34 above, which is incorporated by reference.

However, C2 fails to expressly teach that adjusting the frequency of the processor requires new memory timings.

Kao clearly teaches in the Background (1:20-30) that: "The external frequency is the speed at which the cache and the main memory communicate with the CPU. Changing the external frequency means to change the bus speed. Increase the external frequency one step at a time is the most successful way to overclock a CPU."

Later on Kao teaches that one of the steps of overclocking a CPU may involve (step 8, 2:8-9) "Try some other memory timings in the BIOS setup, if necessary".

Therefore, Kao clearly teaches that changing the external frequency is the most effective manner to overclock the CPU, and if the operating speed of the FSB is changed, clearly that changes the manner in which it interacts with the memory, which **may** therefore involve changing memory timings. In light of the teachings of Kao, It would have been obvious to one of ordinary skill in the art at the time the invention was made that if the processor (and FSB) frequency increased, then memory timings should be re-optimized.

Motivation and rationale is taken from the nature of the reference and the problem to be solved (*Ruiz*, MPEP 2143.01 [R-5], additionally 82 USPQ2d 1385), in that the reference directly addresses the **best** or most successful manner in which to perform the task. Therefore, under the preponderance of the evidence test, as well as under the standards set forth in MPEP 2143.01, (specifically, *In re Fine*; *In re Cartwright*; and particularly *In re Kahn* and 82 USPQ2d 1385), examiner has met the burden of a *prima facie* case against the instant claim.

Conclusion

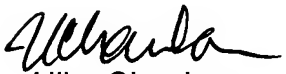
The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Mittal – US 5,719,800 – teaches a dynamic memory speed controller that is configurable by a user.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Woods whose telephone number is 571-272-7775. The examiner can normally be reached on M-F 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Eric Woods 6/8/2007



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